R D ASWIN

Computer Science Undergraduate · Systems & Quantitative Developer

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EDUCATION

Indian Institute of Technology (ISM) Dhanbad 2026 – 2030
Bachelor of Technology (B.Tech) in Computer Science and Engineering

- Focus on low-latency systems programming, deterministic execution architectures, and algorithmic problem solving.
- Relevant Courses: Data Structures & Algorithms, Computer Systems Architecture, Operating Systems, Probability & Stochastic Processes.

Jawahar Navodaya Vidyalaya (JNV) 2019 – 2026
Senior Secondary Education · All India Senior School Certificate Examination

- **JEE Advanced 2026:** All India Rank (AIR) 5,139 (Top 0.3% nationally among 250,000+ qualified candidates).

TECHNICAL SKILLS

Systems & Languages:	Modern C++ (C++20), C, Python, Linux/Unix Shell Scripting (Bash), CMake, GDB, Valgrind, Git
Performance Engineering:	Cache-aligned arena allocation, Zero-allocation hot paths, Lock-free SPSC queues, AVX-512 SIMD vectorization, Profiling (perf)
Distributed & Backend:	WebSockets, Redis (Pub/Sub & Distributed Locks), PostgreSQL, Node.js, TypeScript, Next.js, TCP/UDP sockets

SYSTEMS & QUANTITATIVE ENGINEERING PROJECTS

Low-Latency Limit Order Book (C++20) `C++20 · Linux · CMake · Cache Optimization`
Deterministic Matching Engine & Cache-Aligned Memory Arena (github.com/rd-aswin/limit-order-book)

- **Algorithmic Microstructure:** Engineered a deterministic continuous double-auction matching engine from scratch in Modern C++20 (`-O3 -Wall -Wextra -Wpedantic`) with zero external dependencies.
- **Zero Floating-Point Drift:** Enforced discrete integer fixed-point pricing and strict Price-Time Priority (FIFO) matching, eliminating non-deterministic IEEE-754 floating-point drift across crossing operations.
- **V1 Baseline Architecture:** Implemented Red-Black tree price ladders (`std::map`) and hash lookup tables (`std::unordered_map`), benchmarked via `std::chrono::high_resolution_clock` achieving **~489 ns median tick-to-trade latency** across 100,000 order insertions.
- **V2 Hardware Optimization:** Eliminated dynamic heap allocations and cache misses by pre-allocating a contiguous 1,000,000-order slab arena (`orderPool`), achieving 1ns direct array indexing (`orderPool[orderId]`).
- **64-Byte CPU Cache-Line Packing:** Designed `struct alignas(32) Order` with compact fixed-width types, ensuring **exactly 2 orders occupy a single 64-byte L1 CPU cache line** without split-load straddling.
- **O(1) Intrusive Unlinking:** Embedded `prev_idx` and `next_idx` indices inside `Order`, enabling O(1) order cancellations from resting FIFO queues with zero memory shifting.

Algorithmic Execution & Market Microstructure Testbed `C++20 · Python · Linux`
High-Frequency Burst Generator & Order Routing Simulation Infrastructure

- Engineered high-throughput synthetic order generation harnesses simulating burst liquidity cascades and Poisson arrival distributions to stress-test matching engine throughput under extreme queue depths.
- Integrated automated latency profiling pipelines analyzing nanosecond-resolution P50, P90, P99, and tail latency distributions under heavy market volatility scenarios.

HONORS, COMPETITIONS & MILESTONES

- **Rank #1 — Code[S]sey 3.0:** Champion among all 1st-Year CSE undergraduates at IIT (ISM) Dhanbad in competitive algorithmic programming.
- **Rank 518 (Top 5% Globally) — Jane Street Integral Cup:** Solved high-speed stochastic calculus, integration, and quantitative puzzles.
- **Quantitative Strategist — Indian Student Trading Competition (ISTC 2027):** Modeling algorithmic execution and statistical arbitrage.
- **Founder — Quant Student Syndicate:** Community at IIT Dhanbad focused on algorithmic trading, market microstructure, and C++ systems.
- **Academic STEM Mentor — Govt. of Tamil Nadu:** Selected to mentor students in Advanced Mathematics and Physics problem solving.